AMKOR TECHNOLOGY, INC.
Form 10-K
February 22, 2016

UNITED STATES
SECURITIES AND EXCHANGE COMMISSION
Washington, D.C. 20549
Form 10-K
ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d)
OF THE SECURITIES EXCHANGE ACT OF 1934
For the Fiscal Year Ended December 31, 2015
Commission File Number 000-29472
Amkor Technology, Inc.
(Exact name of registrant as specified in its charter)

Delaware	23-1722724
(State of incorporation)	(I.R.S. Employer Identification Number)

2045 East Innovation Circle
Tempe, AZ 85284
(480) 821-5000
(Address of principal executive offices and zip code)

Securities registered pursuant to Section 12(b) of the Act:

Title of Each Class	Name of Each Exchange on Which Registered
Common Stock, $0.001 par value	The NASDAQ Global Select Market

Securities registered pursuant to Section 12(g) of the Act:
None
Indicate by check mark if the registrant is a well-known seasoned issuer, as defined in Rule 405 of the Securities Act. Yes o No þ
Indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or Section 15(d) of the Act. Yes o No þ
Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934, as amended, during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes þ No o
Indicate by check mark whether the registrant has submitted electronically and posted on its corporate Web site, if any, every Interactive Data File required to be submitted and posted pursuant to Rule 405 of Regulation S-T during the preceding 12 months (or for such shorter period that the registrant was required to submit and post such files). Yes þ No o
Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of registrant’s knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K. o
Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, a non-accelerated filer, or a smaller reporting company. See the definitions of “large accelerated filer,” “accelerated filer” and “smaller reporting company” in Rule 12b-2 of the Exchange Act. (Check one):
Large accelerated filer þ Accelerated filer o Non-accelerated filer o Smaller reporting company o
(Do not check if a smaller reporting company)
Indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Exchange Act). Yes o No þ
The aggregate market value of the voting and non-voting common equity held by non-affiliates of the registrant as of June 30, 2015, based upon the closing price of the common stock as reported by the NASDAQ Global Select Market

on that date, was approximately $591.6 million.

The number of shares outstanding of each of the issuer's classes of common equity, as of January 29, 2016, was as follows: 237,388,425 shares of Common Stock, $0.001 par value.

DOCUMENTS INCORPORATED BY REFERENCE:

Portions of the registrant's Proxy Statement relating to its 2016 Annual Meeting of Stockholders, to be filed subsequently, are incorporated by reference into Part III of this Report where indicated.

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All references in this Annual Report on Form 10-K to "Amkor," "we," "us," "our" or the "company" are to Amkor Technology, Inc. and its subsidiaries. We refer to the Republic of Korea, which is also commonly known as South Korea, as "Korea". All references to "J-Devices" and "Toshiba" are to J-Devices Corporation, our wholly owned subsidiary in Japan, and Toshiba Corporation, respectively. We also refer to our new factory and research and development facility in Korea as "K5". Amounts preceded by ¥ are in Japanese yen. Amkor®, Amkor Technology®, ChipArray®, FusionQuad®, J-Devices®, MicroLeadFrame®, TMV®, SWIFT™, and SLIM™, among others, are trademarks of Amkor Technology, Inc. All other trademarks appearing herein are held by their respective owners. Subsequent use of the above trademarks in this report may occur without the respective superscript symbol (®and ™) in order to facilitate the readability of the report and are not a waiver of any rights that may be associated with the relevant trademarks.

This report contains forward-looking statements within the meaning of the federal securities laws, including but not limited to statements regarding: (1) the amount, timing and focus of our expected capital investments in 2016 including expenditures in support of customer demand in the mobile communications market and expenditures related to our K5 factory and research

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and development facility in Korea, (2) our ability to fund our operating activities for the next twelve months, (3) the effect of changes in capacity utilization on our gross margin, (4) the focus of our research and development activities, (5) the expiration of tax holidays in jurisdictions in which we operate and expectations regarding our effective tax rate and the availability of tax incentives, (6) the creation or release of valuation allowances related to taxes in the future, (7) our repurchase or repayment of outstanding debt or the conversion of debt in the future, (8) payment of dividends, (9) compliance with our covenants, (10) expected contributions to foreign pension plans, (11) liability for unrecognized tax benefits and the potential impact of our unrecognized tax benefits on our effective tax rate, (12) the effect of foreign currency exchange rate exposure on our financial results, (13) the volatility of the trading price of our common stock, (14) changes to our internal controls related to integration of acquired operations and implementation of an enterprise resource planning (“ERP”) system, (15) the anticipated schedule for construction of our K5 factory and research and development facility in Korea, the expansion of our factory in Shanghai, and the transfer of Renesas' Singapore-based automotive microcontroller production to J-Devices, (16) our efforts to enlarge our customer base in certain geographic areas and markets, (17) demand for advanced packages in mobile devices and our technology leadership and potential growth in this market and (18) our expected forfeiture rate for outstanding stock options and restricted shares, (19) our expected rate of return for pension plan assets, (20) demand for advanced System-in-Package ("SiP") modules, (21) our position in the automotive market and (22) other statements that are not historical facts. In some cases, you can identify forward-looking statements by terminology such as “may,” “will,” “should,” “expects,” “plans,” “anticipates,” “believes,” “estimates,” “predicts,” “potential,” “continue,” “intend” or the negative of these other comparable terminology. Because such statements include risks and uncertainties, actual results may differ materially from those anticipated in such forward-looking statements as a result of various factors, including those set forth in the following report as well as in Part I, Item 1A of this Annual Report on Form 10-K.

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PART I

Item 1. Business

OVERVIEW

Amkor is one of the world’s leading providers of outsourced semiconductor packaging and test services. Amkor pioneered the outsourcing of semiconductor packaging and test services through a predecessor corporation in 1968, and over the years we have built a leading position by:

- Designing and developing innovative packaging and test technologies;
- Offering a broad portfolio of cost-effective solutions and services;
- Successfully penetrating strategic end markets which offer solid growth prospects;
- Cultivating long-standing relationships with our customers, which include many of the world’s leading semiconductor companies;
- Collaborating with customers, original equipment manufacturers (“OEMs”) and equipment and material suppliers;
- Developing a competitive cost structure with disciplined capital investment;
- Building expertise in high-volume manufacturing processes and developing a reputation for high quality and solid execution and
- Providing a geographically diverse operating base, with research and development, engineering support and production capabilities at various facilities in China, Japan, Korea, Malaysia, the Philippines and Taiwan.

Our packaging and test services are designed to meet application and chip specific requirements including the type of interconnect technology employed; size; thickness and electrical, mechanical and thermal performance. We are able to provide turnkey packaging and test services including semiconductor wafer bump, wafer probe, wafer backgrind, package design, packaging, test and drop shipment services. Our customers use us for one or more of these services.

We provide our services to integrated device manufacturers (“IDMs”), “fabless” semiconductor companies and contract foundries. IDMs generally design, manufacture, package and test semiconductors in their own facilities. However, the availability of technologically advanced outsourced manufacturing services has encouraged IDMs to outsource a portion of their manufacturing. Fabless semiconductor companies do not have factories and focus exclusively on the semiconductor design process and outsource virtually every step of the manufacturing process. Fabless semiconductor companies utilize contract foundries to manufacture their semiconductors in wafer form, and companies such as Amkor for their packaging and test needs. Some companies will engage a contract foundry to manage the complete semiconductor manufacturing process, and in turn, the contract foundry will outsource some of its packaging and test needs.

Our IDM customers include: Infineon Technologies AG; Intel Corporation; Micron Technology, Inc.; Renesas Electronics Corporation; STMicroelectronics N.V.; Texas Instruments Incorporated and Toshiba Corporation. Our fabless customers include: Avago Technologies; Broadcom Corporation and Qualcomm Incorporated. Our contract foundry customers include: GlobalFoundries Inc. and Taiwan Semiconductor Manufacturing Company Limited.

J-Devices Corporation

On December 30, 2015, we increased our ownership in J-Devices Corporation from 65.7% to 100% through the exercise of existing options. As a result, our accounting for J-Devices changed from the equity method to the consolidation method effective at the time of acquisition.

J-Devices is the largest provider of outsourced semiconductor packaging and test services in Japan with net sales of $0.8 billion in 2015. J-Devices' business covers a broad range of packaging and test services focused on the

automotive, industrial and consumer end markets.

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J-Devices was formed in 2009 as a result of a joint venture between Amkor, Toshiba and J-Devices' predecessor, Nakaya Microdevices Corporation ("NMD"). As part of this transaction, J-Devices acquired certain assets and business, including technology development, of Toshiba's semiconductor packaging business. Since that time, J-Devices has experienced considerable growth through various acquisitions, including the purchase of three packaging and test facilities from Fujitsu Semiconductor Limited in 2012, the purchase of three additional packaging and test facilities from Renesas Electronics Corporation in 2013 and the purchase of our previously wholly-owned subsidiary engaged in semiconductor packaging and test operations in Japan in 2014.

AVAILABLE INFORMATION

Amkor files annual, quarterly and current reports, proxy statements and other information with the U.S. Securities and Exchange Commission (the “SEC”). You may read and copy any document we file at the SEC’s Public Reference Room, 100 F Street, NE, Washington, D.C. 20549. Please call the SEC at 1-800-SEC-0330 for information on the Public Reference Room. The SEC maintains a web site that contains annual, quarterly and current reports, proxy statements and other information that issuers (including Amkor) file electronically with the SEC. The SEC’s web site is http://www.sec.gov.

Amkor’s web site is http://www.amkor.com. Amkor makes available free of charge through its web site, our annual reports on Form 10-K; quarterly reports on Form 10-Q; current reports on Form 8-K; Forms 3, 4 and 5 filed on behalf of directors and executive officers and any amendments to those reports filed or furnished pursuant to the Securities Exchange Act of 1934, as amended, as soon as reasonably practicable after such material is electronically filed with, or furnished to, the SEC. We also make available, free of charge, through our web site, our Corporate Governance Guidelines, the charters of the Audit Committee, Nominating and Governance Committee and Compensation Committee of our Board of Directors, our Code of Business Conduct, our Code of Ethics for Directors and other information and materials. The information on Amkor’s web site is not incorporated by reference into this report.

INDUSTRY BACKGROUND

Semiconductor devices are the essential building blocks used in most electronic products. As electronic and semiconductor devices have evolved, several important trends have emerged that have fueled the growth of the overall semiconductor industry, as well as the market for outsourced semiconductor packaging and test services. These trends include:

- An increasing demand for mobile and home internet-connected devices, including the world-wide adoption of mobile “smart” phones and tablets that can access the internet and provide multimedia capabilities.
- An increase in mobility and connectivity capabilities and growing digital content driving demand for new broadband wired and wireless networking equipment.
- The proliferation of semiconductor devices into well-established end products such as automotive systems due to increased use of electronics for safety, navigation, fuel efficiency, emission reduction and entertainment systems.
- An overall increase in the semiconductor content within electronic products to provide greater functionality and higher levels of performance.
- The growth of advanced System-in-Package ("SiP") modules where multiple semiconductor components with different functionalities are combined into a single integrated circuit ("IC") package. The increasing demand for miniaturization and higher functionality at competitive cost is driving the adoption of advanced SiP in new products.

Our business is impacted by market conditions in the semiconductor industry, which is cyclical by nature and impacted by broad economic factors, such as world-wide gross domestic product and consumer spending. Historical trends indicate there has been a strong correlation between world-wide gross domestic product levels, consumer spending and semiconductor industry cycles.

Outsourcing Trends in Semiconductor Manufacturing

Semiconductor companies outsource their packaging and test needs to service providers such as Amkor for the following reasons:

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Packaging and test service providers have developed expertise in advanced technologies.

Semiconductor packaging and test technologies continue to become more sophisticated, complex and customized due to increasing demands for miniaturization, greater functionality, lower power consumption and improved thermal and electrical performance. This trend has led many semiconductor companies and OEMs to view packaging and test as enabling technologies requiring sophisticated expertise and technological innovation. Many of these companies are also relying on packaging and test service providers as key sources for new package designs and advanced interconnect technologies, thereby enabling them to reduce their internal research and development costs.

Packaging and test service providers offer a cost effective solution in a highly cyclical, capital intensive industry.

The semiconductor industry is cyclical by nature and impacted by broad economic factors, such as changes in worldwide gross domestic product and consumer spending. Semiconductor packaging and test are complex processes requiring substantial investment in specialized equipment, factories and human resources. As a result of this cyclicality and the large investments required, manufacturing facilities must operate at consistently high levels of utilization to be cost effective. Shorter product life cycles, coupled with the need to update or replace packaging and test equipment to accommodate new package types, make it more difficult for integrated semiconductor companies to maintain cost effective utilization of their packaging and test assets throughout semiconductor industry cycles. Packaging and test service providers, on the other hand, can typically use their assets to support a broad range of customers, potentially generating more efficient use of their production assets and a more cost effective solution.

Packaging and test service providers can facilitate a more efficient supply chain and help shorten time-to-market for new products.

We believe that semiconductor companies, together with their customers, are seeking to shorten the time-to-market for their new products, and that having an effective supply chain is a critical factor in facilitating timely and successful product introductions. Packaging and test service providers have the resources and expertise to timely develop their capabilities and implement new packaging technology in volume. For this reason, semiconductor companies and OEMs are leveraging capabilities of packaging and test service providers to deliver their new products to market more quickly.

High quality packaging and test service providers enable semiconductor manufacturers to focus their resources on semiconductor design and wafer fabrication.

As semiconductor process technology migrates to larger wafers and smaller feature sizes, the cost of building a state-of-the-art wafer fabrication factory has risen significantly and can now be several billions of dollars. The high cost of investing in next generation silicon technology and equipment is causing many semiconductor companies to adopt or maintain a “fabless” or “fab-lite” strategy to reduce or eliminate their investment in wafer fabrication and associated packaging and test operations. As a result, these companies are increasing their reliance on outsourced providers of semiconductor manufacturing services, including packaging and test.

STRATEGY AND COMPETITIVE STRENGTHS

Strategy

Our financial goals are sales growth and improved profitability, and we are focusing on the following strategies to achieve these goals:

Leverage Our Investment in Services for Advanced Technologies

We are an industry leader in developing and commercializing cost-effective advanced packaging and test technologies. These advanced technology solutions provide increased value to our customers while typically generating gross margins above our corporate average. This is particularly true in the mobile device market, where growth has outpaced the semiconductor industry rate. An important factor for success in the advanced packaging and test area is to generate reasonably quick returns on investments made for customers seeking leading edge technologies.

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In recent years we have made significant investments in state-of-the-art facilities and equipment to provide services for the industry's most complex devices. With approximately 475 employees engaged in research and development in 2015 focusing on the design and development of new semiconductor packaging and test technologies, we are a technology leader in areas such as fine pitch bumping, advanced flip chip and wafer-level processing. During 2015, we had success capitalizing on our advanced technology to achieve design wins and new product introductions in areas such as chips fabricated at 16 nanometer geometries and advanced SiP products including radio frequency ("RF"), front end modules and micro-electro-mechanical systems ("MEMS") devices.

We work closely with our customers to develop cost-effective leading-edge packages for the next generation of devices, and are making substantial progress in a number of areas. These include Silicon Wafer Integrated Fan-out Technology ("SWIFT") and Silicon-Less Integrated Module ("SLIM") solutions which enable very thin, very small products combining application processors, memory, baseband and other peripheral IC's. They also include packages utilizing Through Silicon Via ("TSV") interconnects and silicon interposers which enable the integration of high performance chips such as high bandwidth memory and graphics processors into a single package.

We believe that the value added by advanced packaging services will continue to grow as our customers and leading electronics OEMs strive for smaller device geometries, higher levels of speed and performance and lower power consumption. We intend to continue to leverage our investment in advanced technology to meet the demand for these services.

Improve Utilization of Existing Assets and Broaden Our Customer Base

Another key to our success is to improve the utilization of our existing assets. The transition by leading edge customers to newer packaging and test equipment platforms typically frees up capacity in existing, previously installed equipment. As part of our strategy, we are focused on developing a second wave of customers to more effectively utilize these assets over a longer period of time. In particular, we have a concerted effort to increase our sales to Chinese and Taiwanese fabless chip companies, since they have a significant portion of the mid-tier and entry-level segments of the mobile device market where much of the growth is occurring.

In 2015, we established a dedicated Greater China Business Unit, opened new sales offices in Shanghai, Beijing and Shenzhen, and continued hiring new salespeople, design engineers and customer service personnel to assist our customers in China.

Another key part of our Greater China strategy is our regional manufacturing footprint, particularly our world-class factory in Shanghai. We are building an addition to this facility, which will expand our clean room space by nearly 45%, to a total of roughly 625,000 square feet. Our Shanghai facility serves international and local customers, with a heavy emphasis on wafer-level packaging, wafer bumping, stacked die packaging and advanced test services.

Selectively Grow Our Scale and Scope through Strategic Investments

From time to time we see attractive opportunities to grow our customer base and expand markets through strategic investments. For example, in 2015 we completed the acquisition of 100% of J-Devices, our outsourced semiconductor assembly and test ("OSAT") joint venture in Japan. We believe that with this acquisition we have become the largest OSAT by revenue for the automotive market, with roughly $750 million in combined automotive-based revenues in 2015. In addition, Renesas agreed to transfer most of its Singapore-based automotive microcontroller production to J-Devices' factories. That transfer began in 2015 and will be completed in 2016.

We believe that selective growth through joint ventures, acquisitions and other strategic investments can help diversify our revenue streams, improve our profits and maintain our technological leadership.

Competitive Strengths

The outsourced semiconductor packaging and test market is very competitive. We also compete with the internal semiconductor packaging and test capabilities of many of our customers and foundries. We believe we are well-positioned

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in the outsourced packaging and test services market. The following competitive strengths allow us to build upon our industry position and to remain one of the preferred providers of semiconductor packaging and test services.

Leading Technology Innovator

We are a leader in developing advanced semiconductor packaging and test solutions. We have designed and developed several state-of-the-art package formats and technologies including our Package-on-Package ("PoP") platform with Through Mold Via ("TMV") technology, FusionQuad, flip chip ball grid array, multi-chip modules with a silicon interposer placed between the module chips and substrate, copper pillar bumping and fine pitch copper pillar flip chip packaging technologies. In addition, we believe that as semiconductor technology continues to achieve smaller device geometries with higher levels of speed and performance, packages will increasingly require wafer-level chip scale packaging, flip chip and advanced integrated and modular interconnect solutions that combine multiple active chips and other elements in a single package. We have been investing in our technology leadership in wafer bumping, wafer-level processing, advanced SiP, SLIM and SWIFT packaging technologies. We have also been a leader in developing environmentally friendly integrated circuit packaging, which involves the elimination of lead and certain other materials.

The semiconductor industry is now in a period of packaging development where integrated wafer-level fan-out and TSV interconnect technologies will be used to create the next generation of advanced packages. We continue to invest in developing the key processes and packaging and test technologies required for our customers to deliver advanced integrated and modular solutions to market. We are a leader in wafer thinning, micro-bumping and TSV-based flip chip innovation, and we are leveraging our technology development relationships with key customers in diverse applications to develop and deploy these packaging and test solutions.

Long-Standing Relationships and Collaboration with Prominent Semiconductor Companies

Our customers include most of the world's largest semiconductor companies and over the last four decades, we have developed long-standing relationships with many of these companies. We believe that our production excellence has been a key factor in our success in attracting and retaining customers. We work with our customers and our suppliers to develop proprietary process technologies to enhance our existing capabilities, reduce time-to-market, increase quality and lower costs.

We believe that our focus on research and product development will enable us to enter new markets early, capture market share and promote the adoption of our new package designs as industry standards. We collaborate with customers and leading OEMs to develop comprehensive packaging solutions that make it easier for next-generation semiconductors to be designed into next-generation end products. By collaborating with leading semiconductor companies and OEM electronic companies, we gain access to technology roadmaps for next generation semiconductor designs and obtain the opportunity to develop new packages that satisfy their future requirements.

Broad Offering of Semiconductor Package Design, Packaging and Test Services

Creating successful interconnect solutions for advanced semiconductor devices often poses unique thermal, electrical and mechanical design challenges, and we employ a large number of engineers to solve these challenges. We provide services for a wide variety of products. This wide variety of packaging offerings is necessary to meet the diverse needs of our customers for the optimal combination of performance, size and cost attributes. Our solutions enable our customers to focus on semiconductor design and wafer fabrication while utilizing Amkor as their turnkey design, packaging and test services provider and, in many cases, their packaging technology innovator.

We also offer an extensive line of advanced probe and final test services for analog, digital, logic, mixed signal and RF semiconductor devices. We believe that the breadth of our design, packaging and test services is important to customers seeking to limit the number of their suppliers.

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Geographically Diversified Operating Base

We have a broad and geographically diversified operating footprint strategically located in six countries in many of the world's important electronics manufacturing regions. We believe that our scale and scope allow us to provide cost effective solutions to our customers by:

- Offering capacity to absorb large orders and accommodate quick turn-around times;
- Obtaining favorable pricing on materials and equipment, where possible, by using our purchasing power and leading industry position;
- Qualifying production of customer devices at multiple manufacturing sites to mitigate the risks of supply disruptions and
- Providing capabilities and solutions for customer-specific requirements.

For financial information about geographic areas, see Note 18 to our Consolidated Financial Statements in Part II, Item 8 of this Annual Report on Form 10-K.

Competitive Cost Structure and Disciplined Capital Investment

There is a continuous push throughout the entire semiconductor supply chain for lower cost solutions. We work to maintain a competitive cost structure and make disciplined capital investment decisions so that we can provide cost-competitive solutions to our customers and achieve sustainable profitability and cash flow. Some of our cost control efforts have included: (1) improving the utilization of our existing assets; (2) increasing strip densities to drive higher throughput; (3) migrating from gold wire to copper wire for certain wirebond packages and (4) increasing labor productivity.

We operate in a cyclical industry. During an industry downturn we seek to reduce our costs and drive greater factory and administrative efficiencies. Cost control efforts can include reducing labor costs by temporarily lowering compensation, reducing employee and contractor headcount, shortening work weeks and obtaining labor-related foreign government subsidies where available.

PACKAGING AND TEST SERVICES

Overview of Semiconductor Manufacturing Process

In general, the semiconductor manufacturing process consists of integrated circuit design, wafer fabrication, wafer probe, packaging and final test.

Integrated circuit design involves the laying out of electronic components, such as transistors, resistors, capacitors and the metallic interconnect of these components, to achieve the desired device functionality. Wafer fabrication is a multiple-step sequence of photolithographic and chemical processing steps during which the integrated circuits are gradually created on semiconductor material, typically a silicon wafer. Individual integrated circuits are generally known as a “chip” or “die”, and a single wafer will contain many die. Wafers are fabricated by two types of companies - IDMs which design and fabricate wafers using their own in-house manufacturing facilities, and contract foundries which manufacture wafers that are designed by fabless companies or other customers.

The packaging and test services we provide occur subsequent to wafer fabrication. The wafers that we receive from our customers are generally consigned to us; we do not own the consigned wafers or record their value in our financial statements. During wafer probe, each individual die is electrically tested, or probed, for defects. Packaging is the processing of bare die to facilitate electrical connections and heat dissipation and protect the die. The wafer is separated into individual die. Each good die is then assembled into a package that typically encapsulates the die for

protection and creates the electrical connections used to connect the package to a printed circuit board, module or other part of the electronic device. In some packages, chips are attached to a substrate or leadframe carrier through wirebonding or flip chip interconnects and then encased in a protective material. Or, for a wafer-level package, the electrical interconnections are created directly on the surface of the die (while the wafer is still intact) so that the chip may be attached directly to other parts of an electronic

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device without a substrate or leadframe. The packages are then tested using sophisticated equipment to ensure that each packaged chip meets its design and performance specifications.

Packaging and Test Technologies and Processes

Our packages employ wirebond, flip chip, copper clip and other interconnect technologies. We use leadframe and substrate package carriers, and we perform a variety of test services.

Interconnect Technologies

Wirebond: In packages that employ wirebond interconnect technology, the die is mounted face up on the package carrier and the interconnections between the die and package carrier are made through very fine gold, silver or copper wires which are attached from the bond pads of the die to the package carrier. Wirebonding is generally considered to be the most cost-effective and flexible interconnect technology and is used to assemble the majority of semiconductor packages.

Flip Chip: In packages that employ flip chip interconnect technology, the interconnections between the die and package carrier are made through conductive “bumps” that are placed directly on the die surface utilizing a process called wafer bumping. The bumped die is then “flipped over” and placed face down, with the bumps connecting directly to the package carrier. Flip chip allows a higher number of interconnects than wirebond as it uses the entire surface area of the die, and sometimes the perimeter as well, instead of just the perimeter as used by most wirebond packages. Flip chip also provides enhanced thermal and electrical performance, and enables smaller die and thinner, smaller form factors (or physical package dimensions).

The wafer bumping process consists of preparing the wafer for bumping and forming or placing the bumps. Preparation may include cleaning, removing insulating oxides and providing a pad metallurgy that will protect the interconnections while making good mechanical and electrical connection between the bump and the wafer.

Copper Clip: Copper clip interconnect technology uses a solid copper bridge or “clip” to connect the die to the package carrier. The clip allows a higher level of current flow than a wire and also provides a better method of heat transfer from the die. The clip is either spot welded, or more often re-flow soldered, to the die pads and the package carrier pads.

Package Carriers

Leadframe: A leadframe is a miniature sheet of metal, generally made of copper and silver alloys, on which a pattern of electrical connections (or “leads”) has been cut. The leads are generally placed around the perimeter of the leadframe and are used to connect the package to the system board. The number of leads on an individual leadframe is limited as electrical shorting can occur if the leads are placed too close together.

Substrate: A substrate is a laminate of multiple layers of epoxy resin, woven glass fibers and metal conductors. Bumps provide the electrical connection to the system board. The bumps are typically distributed evenly across the bottom surface of the substrate (called a “ball grid array” format). This allows greater distance between individual leads and a higher number of interconnects than leadframe packages.

Test Services

Amkor provides a complete range of semiconductor testing services including wafer testing or probe and final test. We offer a full range of test software, hardware, integration and product engineering services, and we support a range

of business models and test capabilities. Substantially all of our test business is derived from testing packages that we assemble.

Wafer Test Services: Wafer test, also referred to as wafer probe, is performed after wafer fabrication or wafer bumping to screen out defective devices prior to packaging. We offer a range of wafer test coverage that can be tailored based on the cost and complexity of the die, the package and the product. These services range from coarse level screening for major defects all the way up to probing at high digital speeds and can include full radio frequency transmit and receive as well as testing at multiple temperatures. Wafer testing can also involve a range of wafer mapping and inspection operations.

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Final Test Services: After the packaging process, final test is performed to ensure that the packaged device meets the customer's requirements. Final test spans a range of rigor and complexity depending on the device and end market application. More rigorous types of final test include testing multiple times under different electrical and temperature conditions and before and after device reliability stresses, such as burn-in. In addition to electrical testing, specialized solutions are required for packages that also process non-electric stimuli.

The electrical tests are a mix of functional, structural and system-level tests depending on the customer's requirements and cost and reliability parameters. The electrical test equipment we use includes commercially available automated test equipment, customized and proprietary system level test equipment and innovative types of low cost test equipment developed by Amkor.

Advanced Products and Mainstream Products

We offer a broad range of advanced and mainstream packaging and test services to our customers. We refer to our flip chip, wafer-level processing and related test services as "Advanced Products", and our wirebond packaging and related test services as "Mainstream Products". The following table sets forth, for the periods indicated, the amount of advanced and mainstream packaging and test net sales and the percentage of such net sales (excluding J-Devices):

	Year Ended December 31,								
	2015			2014			2013		
	(In millions, except percentage of net sales)								
Advanced products	$1,433	49.7	%	$1,553	49.6	%	$1,451	49.1	%
Mainstream products	1,452								